WHAT IS CLAIMED IS:

1. A data processor comprising:

C execution clusters, each of said C execution clusters comprising an instruction execution pipeline having N processing stages capable of executing instruction bundles comprising from one to S syllables, wherein each said instruction execution pipelines is L lanes wide, each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles;

an instruction cache capable of storing a plurality of cache lines, each of said cache lines comprising C*L syllables;

an instruction issue unit capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said C execution clusters; and

alignment and dispersal circuitry capable of receiving said complete instruction bundles from said instruction issue unit and routing each said received complete instruction bundles to a correct one of said C execution clusters as a function of at least one address bit associated with each of said complete instruction bundles.

2. The data processor as set forth in Claim 1 wherein said alignment and dispersal circuitry routs each said received complete instruction bundles to said correct execution cluster as a function of at least one address bit associated with at least one syllable in said each complete instruction bundle.

3. The data processor as set forth in Claim 1 wherein said alignment and dispersal circuitry routes each received complete instruction bundles to said correct execution cluster as a function of a cluster bit associated with each complete instruction bundle.

4. The data processor as set forth in Claim 1 wherein said alignment and dispersal circuitry routs each said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in said each complete instruction bundle.

5. The data processor as set forth in Claim 1 wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing said each received complete instruction bundle to any one of said C execution clusters.

6. The data processor as set forth in Claim 5 wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry.

7. The data processor as set forth in Claim 6 wherein said control logic circuitry controls said multiplexer circuitry as a function of at least one of:

1) said at least one address bit associated with said each complete instruction bundle;

2) at least one address bit associated with at least one syllable in said each complete instruction bundle; and

3) a cluster bit associated with said each complete instruction bundle.

8. The data processor as set forth in Claim 1 wherein L=4.

9. The data processor as set forth in Claim 1 wherein C=3.

10. A processing system comprising:

a data processor;

a memory coupled to said data processor;

a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor, wherein said data processor comprises:

C execution clusters, each of said C execution clusters comprising an instruction execution pipeline having N processing stages capable of executing instruction bundles comprising from one to S syllables, wherein each said instruction execution pipelines is L lanes wide, each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles;

an instruction cache capable of storing a plurality of cache lines, each of said cache lines comprising C*L syllables;

an instruction issue unit capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said C execution clusters; and

alignment and dispersal circuitry capable of

receiving said complete instruction bundles from said instruction issue unit and routing each said received complete instruction bundles to a correct one of said C execution clusters as a function of at least one address bit associated with each of said complete instruction bundles.

11. The processing system as set forth in Claim 10 wherein said alignment and dispersal circuitry routs each said received complete instruction bundles to said correct execution cluster as a function of at least one address bit associated with at least one syllable in said each complete instruction bundle.

12. The processing system as set forth in Claim 10 wherein said alignment and dispersal circuitry routs each said received complete instruction bundles to said correct execution cluster as a function of a cluster bit associated with said each complete instruction bundle.

13. The processing system as set forth in Claim 10 wherein said alignment and dispersal circuitry routs each said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in said each complete instruction bundle.

14. The processing system as set forth in Claim 10 wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing said each received complete instruction bundle to any one of said C execution clusters.

15. The processing system as set forth in Claim 14 wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry.

16. The processing system as set forth in Claim 15 wherein said control logic circuitry controls said multiplexer circuitry as a function of at least one of:

1) said at least one address bit associated with said each complete instruction bundle;

2) at least one address bit associated with at least one syllable in said each complete instruction bundle; and

3) a cluster bit associated with said each complete instruction bundle.

17. The processing system as set forth in Claim 10 wherein L=4.

18. The processing system as set forth in Claim 10 wherein C=3.

19. For use in a data processor comprising C execution clusters, each of the C execution clusters comprising an instruction execution pipeline having N processing stages capable of executing instruction bundles comprising from one to S syllables, wherein each the instruction execution pipelines is L lanes wide, each of the L lanes capable of receiving one of the one to S syllables of the instruction bundles, a method of routing instruction bundles into the L lanes in the C execution clusters comprising the steps of:

fetching cache lines from an instruction cache, each of the cache lines comprising C*L syllables;

issuing complete ones of the instruction bundles toward the C execution clusters; and

routing each the received complete instruction bundles to a correct one of the C execution clusters as a function of at least one of:

1) the at least one address bit associated with the each complete instruction bundle;

2) at least one address bit associated with at least one syllable in the each complete instruction bundle; and

3) a cluster bit associated with the each complete instruction bundle.

20. The method as set forth in Claim 19 wherein L=4 and C=3.